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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,489	04/15/2004	Frederic Reblewski	003921.00008	6574

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EXAMINER	
SAXENA, AKASH	
ART UNIT	**PAPER NUMBER**
2128	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/824,489	REBLEWSKI, FREDERIC	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claim(s) 1-13 has/have been presented for examination based on amendment filed on 29th January 2007
2. Claim(s) 11-13 is/are amended.
3. Claim(s) 14 is/are cancelled.
4. *Amended claim(s)* 12 & 13 are rejected under 35 USC § 112 ¶1st.
5. Claim(s) 1-13 remain rejected under 35 USC § 102 as anticipated by Barbier. Clarified mapping is provided to claims 1 in view of applicant's remarks. Claims 11-13 are amended and respective and responses are provided likewise.
6. The arguments submitted by the applicant have been fully considered. Claims 1-13 remain rejected and this action is made FINAL. The examiner's response is as follows.

Claim Rejections - 35 USC § 112 ¶1st

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. *Amended claims 12-13* are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding Claim 12

Claim 12 discloses the limitation

> prior to the step (b) of routing the output through a first reconfigurable interconnect stage, routing the output from the first simulation processor through a third reconfigurable interconnect stage

Where as no support or mapping for the claim language can be found in the specification or the drawing for this limitation.

Regarding Claim 13

Examiner is unable to find support for the updated sequence of limitations in the disclosure as both the limitations in this claim are configuring the first reconfigurable interconnect stage. Examiner requests the applicant to particularly point out where each limitation is taught.

Claim Rejections - 35 USC § 112 ¶2nd

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 13

Claim 13 further is unclear as to specifically how the sequence of steps is performed and no support appears to be present for this limitation. Both the limitations in this claim appear to be drawn to only the first reconfigurable interconnect stage. Clarification is requested.

Response to Applicant's Remarks for 35 U.S.C. § 102

9. Claim 1-14 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,574,388 issued to Barbier et al (Barbier hereafter).

Regarding Claim 1-14

Applicant has argued that Barbier does not anticipate the limitations presented in the claim. Specifically, the element 113 (Fig.3) is not a bridge but instead an in/out switch.

Examiner respectfully disagrees. Barbier does not limit the element 113 as suggested by the applicant. Even if the reference is interpreted as suggested by applicant, Barbier anticipates the claimed invention. Examiner has now clarified the mapping in view of applicant's arguments.

Responsive to applicant's argument that the mapping is not as intended by claims amounts to a recitation of the intended use of the claimed invention which must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. *If the prior art structure is capable of performing the intended use, then it meets the claim.* In this instance, the claimed invention uses multiple crossbar switches, some of which feedback (3rd crossbar feeding back to 2nd crossbar switch). This feature is anticipated by the 3 levels of crossbar in the prior art (Barbier: Fig.6a).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claim 1-13 rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,574,388 issued to Barbier et al (Barbier hereafter).

Regarding Claim 1 (Updated due to remarks for clarification)

Barbier teaches in a logic simulation system (Barbier: Fig.1 col.3 Lines 49-61), a reconfigurable interconnect network (Barbier: Fig.3 & 4a, Col.45 Lines 16-26) comprising a plurality of simulation processors (Barbier: Fig. 3 & 8-10 – Matrix Board having Logic Elements (LE) as simulation processors); a first reconfigurable interconnect stage configurable to receive outputs from the simulation processors (Barbier: *Fig 3 Element 104; Fig 6a*); a second reconfigurable interconnect stage configurable to-receive outputs from the first reconfigurable interconnect stage (Barbier: *Fig. 3 Element 114b; Fig.6a*); and a third reconfigurable interconnect stage configurable to receive outputs from the second reconfigurable interconnect stage (Barbier: *Fig.6a Element 622*), and further configurable to provide outputs to inputs of the second reconfigurable interconnect stage (Barbier: *Fig.6a from Element 622 to 114a*).

Regarding Claim 2 (Updated due to remarks for clarification)

Barbier teaches the second reconfigurable interconnect stage is further configurable to provide outputs to inputs of the simulation processors (Barbier: *Fig.3 Element 114a to 104 to 102* or *Fig.6a Element 114a to 104 to 102*).

Regarding Claim 3

Barbier teaches further including a memory coupled to the second reconfigurable interconnect stage (Barbier: Fig.3), the second reconfigurable interconnect stage being dynamically configured in accordance with a content of the memory (Barbier: Fig.3 & 4a, Col.5 Lines 16-26).

Regarding Claim 4

Barbier teaches a logic simulation system (Barbier: Fig.1 col.3 Lines 49-61), a reconfigurable interconnect network (Barbier: Fig.3 & 4a, Col.45 Lines 16-26) a plurality of clusters, each cluster including plurality of simulation processors (Barbier: Fig.3, Fig.6a and Fig.10). Claim 4 further discloses similar limitations as claim 1 and is rejected for the same reasons.

Regarding Claim 5

Barbier teaches a second reconfigurable interconnect stage is further configurable to provide outputs back to inputs of the simulation engines of the clusters (Barbier: Fig.3 Element 104 to 102; also Fig.6a).

Regarding Claim 6

Claim 6 has similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 7

Claim 7 has similar limitations as claim 2 and is rejected for the same reasons as claim 2.

Regarding Claim 8

Claim 8 is identical to claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 9

Barbier teaches outputs of the second reconfigurable interconnect stage are coupled to the inputs of the third reconfigurable interconnect stage using a butterfly topology (Barbier: Fig.7).

Regarding Claim 10

Barbier teaches the second and third reconfigurable interconnect stages are each a plurality of crossbars (Barbier: Fig.3, 4a; 6b).

Regarding Claim 11 (Updated due to amendment and remarks)

Barbier teaches a method of routing an output from a simulation processor in a reconfigurable interconnect network of a logic simulation system (Barbier: Col.1 Lines 10-12; Fig.1 col.3 Lines 49-61, Fig.3 & 4a, Col.45 Lines 16-26; Fig. 3 & 8-10 – Matrix Board having Logic Elements (LE) as simulation processors) method comprising the following steps in the following order: (a) receiving an output from a first simulation processor (Barbier: Fig. 3 Element 102 to 104); (b) routing the output through a first reconfigurable interconnect stage (Barbier: Fig. 3 Element 102 to 104 to 114a/b); (c) routing the output through a second reconfigurable interconnect stage (Barbier: Fig. 3 Element 114/a/b); (e) routing the output back through the first reconfigurable interconnect stage (Barbier: Fig. 3 Element 114a to 104; Also see Col.5 Lines 10-13); (f) routing the output to a second simulation processor (Barbier: Fig.6a to board I/O Connection and to other FPGA's, e.g. FPGA 23; Alternatively LE Array has plurality of processors – See Crossbar 104 feeding back to 102 LE Array - Col.5 Lines 10-13).

Regarding Claim 12 (Updated due to amendment and remarks)

Barbier teaches does not explicitly teach prior to the step (b) of routing the output through a first reconfigurable interconnect stage, routing the output from the first simulation processor through a third reconfigurable interconnect stage, however, crossbar switches are programmable (Barbier: Col.1 Lines 23-27) and such a routing can be achieved if desirable by making a intervening crossbar switches transparent and that is *common knowledge* in the art.

Regarding Claim 13 (Updated due to amendment and remarks)

Barbier teaches first configuring the first reconfigurable interconnect stage, prior to the step of first routing, *prior to step (b) of routing the output through a first reconfigurable interconnect stage (Barbier: Attached memory Col.4 Lines 42-52)* according to a first configuration; and second configuring the first reconfigurable interconnect stage, prior to the *step (e) routing the output back through the first reconfigurable interconnect stage* and after the *step (b)* of routing *the output through a first reconfigurable interconnect stage;* according to a second configuration (Barrier: Fig.3, 4a and 6a; Col.5 Lines 16-26).

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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